CH503 & CH503C

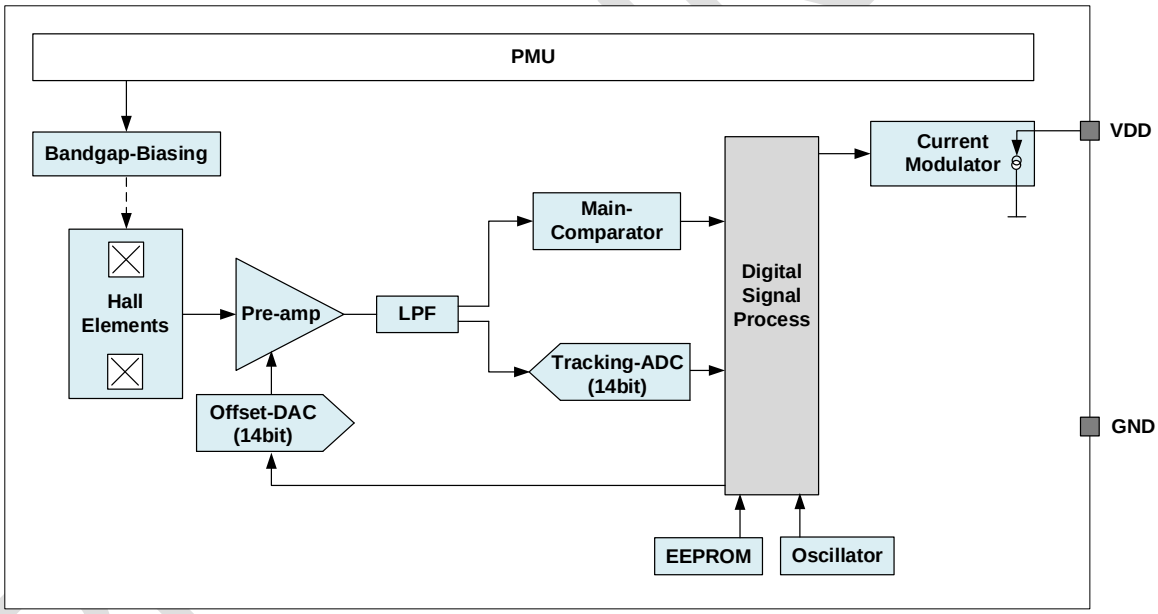
Differential Two-Wire Wheel Speed Sensor IC

Features

- Two-wire current interface
- Integrated capacitor: 1-nF (C version)
- On-chip EEPROM with factory-programming options to optimize performance
- Output variants:
  - CH503 & CH503C: Single pulse (standard protocol)
  - CH504 & CH504C: PWM protocol
  - CH505 & CH505C: AK protocol
- Dynamic self-calibration principle
- Wide operating temperature range: -40°C to 150°C
- Applicable for small pitches, CH503(C): 2-mm hall element distance
- South and north pole pre-induction possible
- Compliant with all requirements in ISO 26262:2018, 8-14 for a component supplier to support safety requirements up to ASIL B

Package

Functional Block (CH503 & CH503C)



General Description

The CH503(C) hall-based wheel speed sensor delivers speed information via a current protocol to vehicle & motorcycle dynamics control systems and Anti-Lock Braking Systems (ABS).

The sensor features a fast power-up time of typical 210us, high sensitivity and excellent jitter performance, enabling secure speed measurement. The device is specified over a wide temperature range of -40 to 150°C, and is designed to meet harsh automotive environment with optimized ESD and EMC performance. For best BCI performance, the CH503C is provided with a 1-nF integrated capacitor.

Revision History

Date	Revision	Change
Nov 2021	0.1	Preliminary
March 2022	0.2	Updated pkg info & format; still need to revise a lot content, draft version
March 2022	0.3	Added leading Tier1 test results
April 2022	0.4	Updated block diagram (EEPROM), power up time typ 210us max 273us; added section 3 function description; updated all graphs and POD

Table of Contents

1 Product Family Members

Part No.	Marking	Description
CH503	C503	Two-wire current interface, CSO-2 package, packing blister carrier tape, QTY TBD, without integrated capacitor
CH503C	C503C	Two-wire current interface, CSO-2 package, packing blister carrier tape, QTY TBD, with integrated capacitor

*See separate datasheets for CH504 and CH505. *目前处于前期样片阶段，为方便备样，丝印暂时是统一的，但会做标签区分。请以原厂沟通的信息为准。

2 Pin Definitions and Descriptions

Pin No.	Name	Type	Function
1	VDD	Supply	Supply voltage
2	GND	Ground	Connect to ground

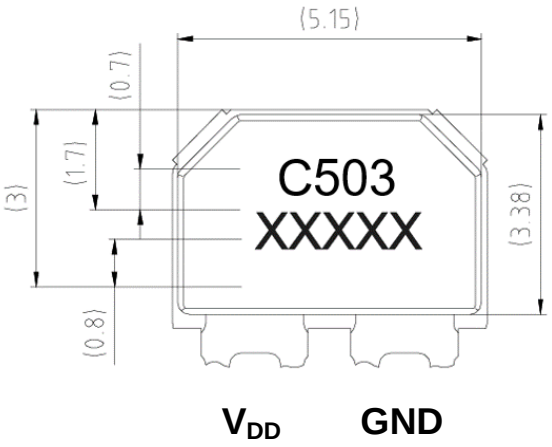


Figure 1 Pin Assignment and Top-Side-Marking of CSO-2 Package

3 Function Description

3.1 General

The CH503(C) detects the motion of active wheels (multiple encoder) and passive wheels (i.e., having ferromagnetic teeth) by measuring the differential flux density of the magnetic field. A back-biasing permanent magnet must be used when pairing with passive wheels. Either south or north pole of the magnet can be attached to the back side of the IC package.

The device is designed with a dynamic self-calibration algorithm to cancel the pre-induction offset (max ± 30mT) between outer probes and mechanical offsets. Max 4 magnetic edges are necessary for self-calibration. After the offset calibration sequence, switching occurs when the input signal crosses the arithmetic mean of its maximum and minimum values.

A valid sensor output can only exist in two states, OFF or ON, which is indicated by LOW and HIGH current consumption respectively.

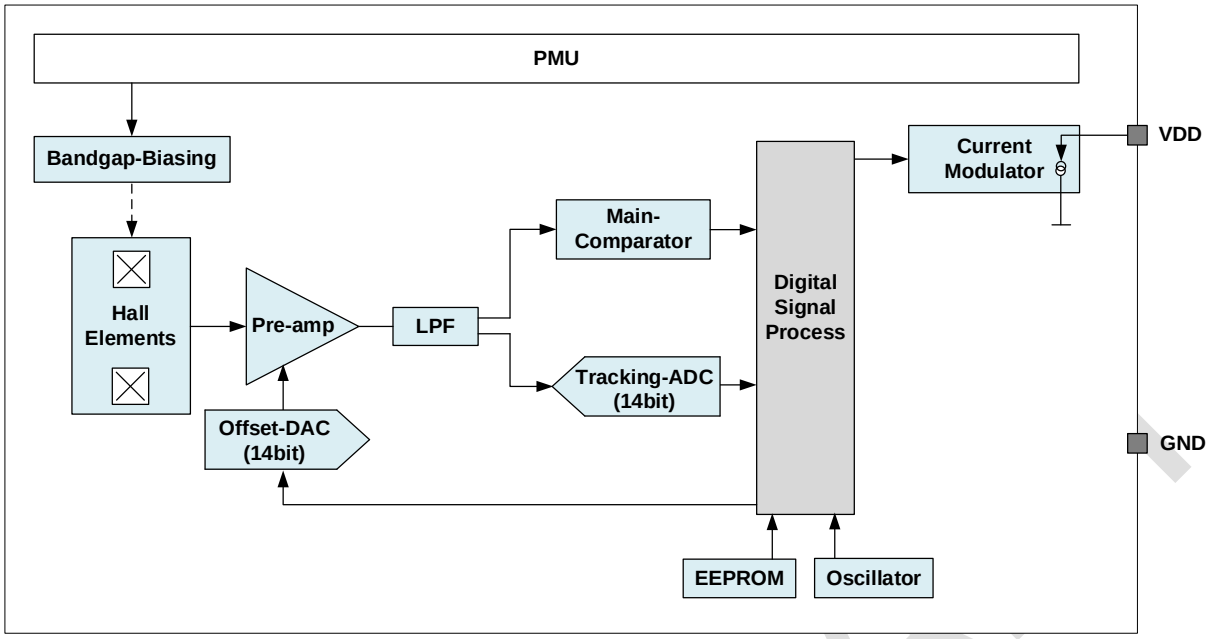


Figure 2 Functional block diagram

The CH503(C) signal path includes a hall element pair, a differential-amp, a low-pass filter, and a comparator feeding a switched current output stage.

The offset cancellation is accomplished with a feedback loop that consists of a 14-bit tracking ADC, a digital signal processor and a 14-bit offset-cancellation DAC.

- The differential input signal is digitized by the tracking ADC and fed into the digital core.
- The arithmetic mean of minimum and maximum values of the input signal is calculated.
- The offset of this mean value is determined and then fed into the offset-cancellation DAC.

Switching occurs at zero-crossing. Once transitioned to the calibrated mode, the offset correction algorithm of the digital core is switched into a low-jitter mode, avoiding oscillation of the offset DAC LSB. Signals below a defined threshold ΔB_{Limit} (Figure 7) are not detected to avoid unwanted parasitic switching.

An on-chip oscillator serves as clock generator for the internal digital core, and a 3-V voltage regulator provides supply internally.

3.2 Uncalibrated mode and calibrated mode

To detect the signal transient, a threshold DNC (digital noise constant) needs to be exceeded. This DNC is determined by the signal amplitude and initial offset value. The smallest DNC (d1 in Figure 3), defines the parameter "$dB_{startup}$".

When the signal slope is identified as a rising-edge (or falling-edge), a trigger pulse will be issued to the current modulator. A 2nd trigger pulse is issued as soon as a falling-edge (or rising-edge respectively) is detected (and vice versa).

A phase shift between the magnetic input signal and output signal occurs, when the digital noise constant value changes (d1 → d2) with the magnetic field amplitude. In the calibrated mode the output will switch at zero-crossing of the input signal. The phase shift between input and output signal is no longer determined by the ratio between DNC and signal amplitude. Therefore, a sudden change in the phase shift may occur during the transition from uncalibrated to calibrated mode. The summed-up change in phase shift from the first output edge issued to the output edges in calibrated mode will not exceed ± 90°. After calibration, consecutive output edges should have a nominal delay of about 180°.

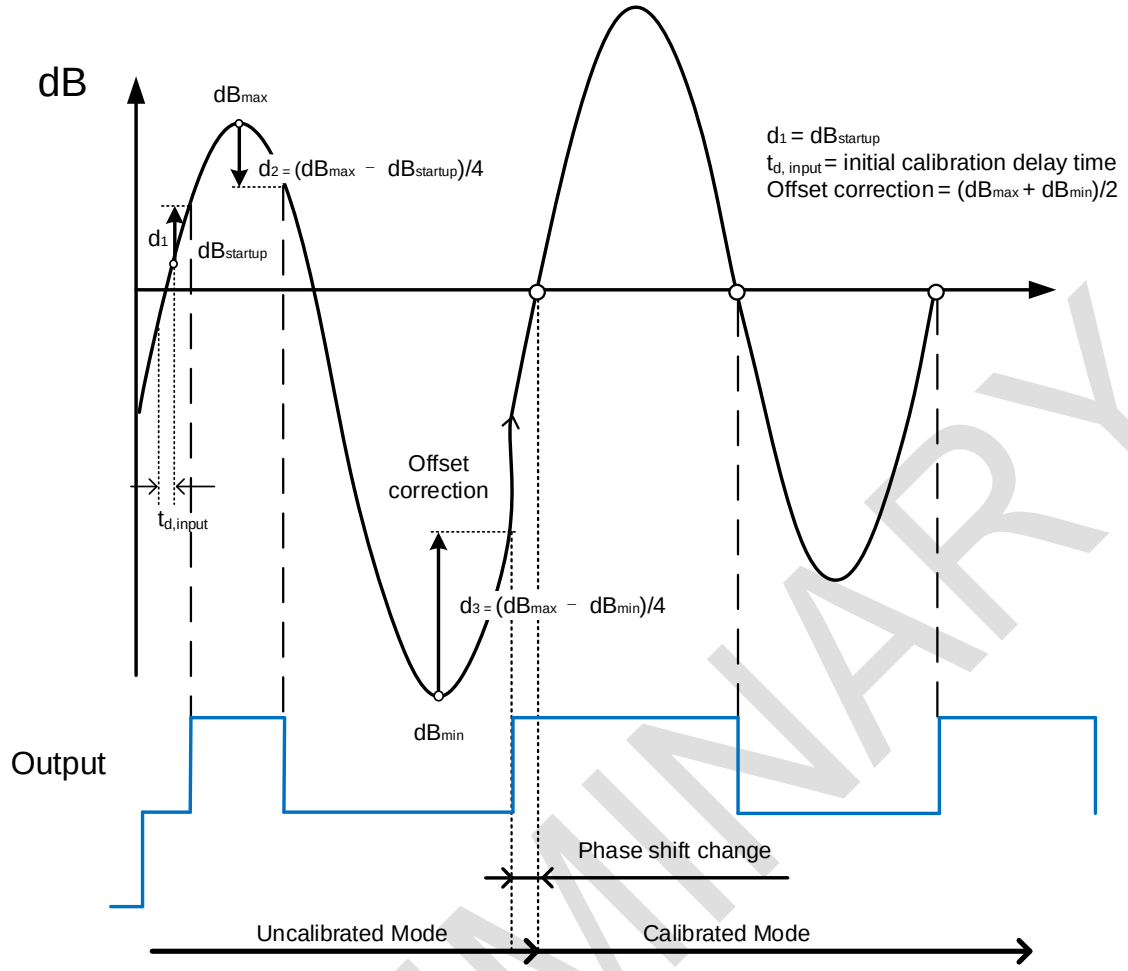


Figure 3 Example of transition from uncalibrated to calibrated mode

3.4 Output description

Ideally, the output shows a duty cycle of 50%. But in real applications, the duty cycle can be affected by the mechanical dimensions of the target wheel and its tolerances (40% to 60% could be exceeded for pitch >> 4mm due to the zero-crossing principle).

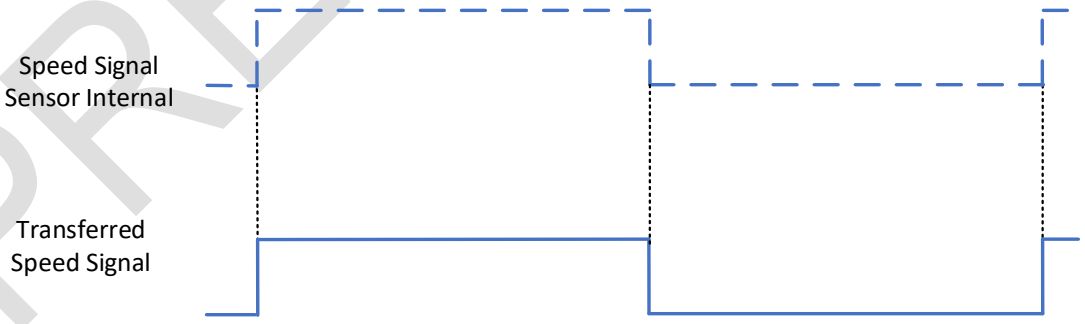


Figure 4 Speed Signal

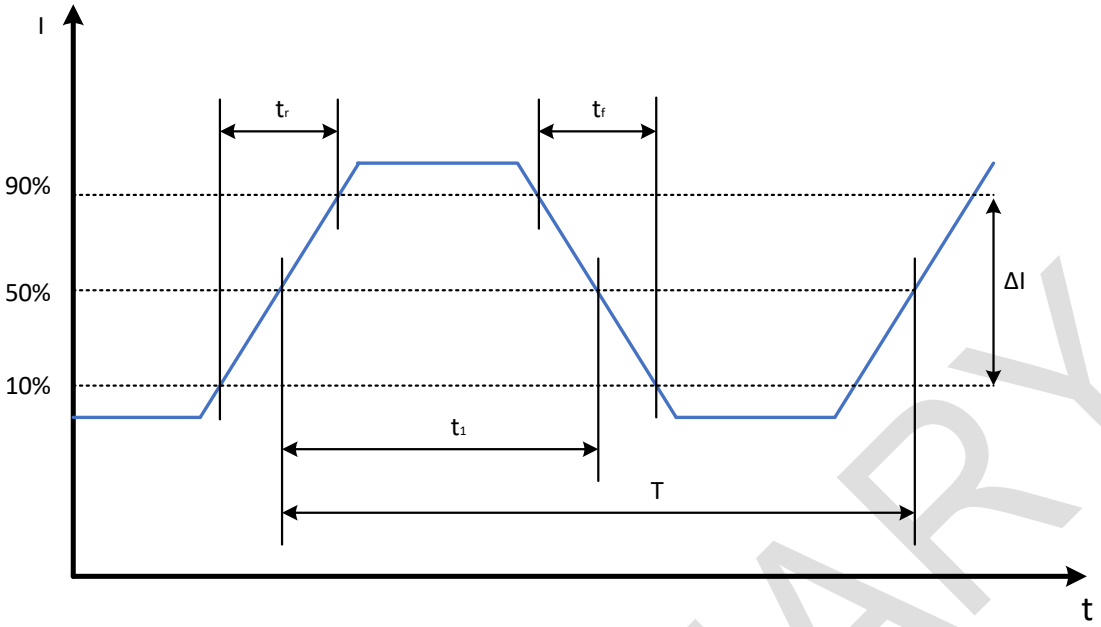


Figure 5 Definition of Rise and Fall Time

3.5 Behavior at magnetic input signals f_{mag} < 1Hz

Magnetic changes exceeding $\Delta\hat{B}_{startup}$ can cause output switching of the CH503(C), even at f_{mag} significantly lower than 1 Hz. Depending on their amplitude, edges slower than $\Delta t_{startup}$ might be detected. If the digital noise constant ($\Delta\hat{B}_{startup}$) is not exceeded before $\Delta t_{startup}$, a new initial self-calibration is started. In other words, $\Delta\hat{B}_{startup}$ needs to be exceeded before $\Delta t_{startup}$. Output switching strongly depends on signal amplitude and initial phase.

3.6 Start-up and under-voltage behavior

The voltage supply comparator has an integrated hysteresis V_{hys} with the maximum value of the release level V_{rel} < 4.5V. This determines the minimum required supply voltage V_{DD} of the chip. A minimum 0.7-V V_{hys} is implemented thus avoiding a toggling of the output when the supply voltage V_{DD} is modulated due to the additional voltage drop at R_M (= 75Ω) when switching from LOW to HIGH current level and V_{DD} = 4.5V.

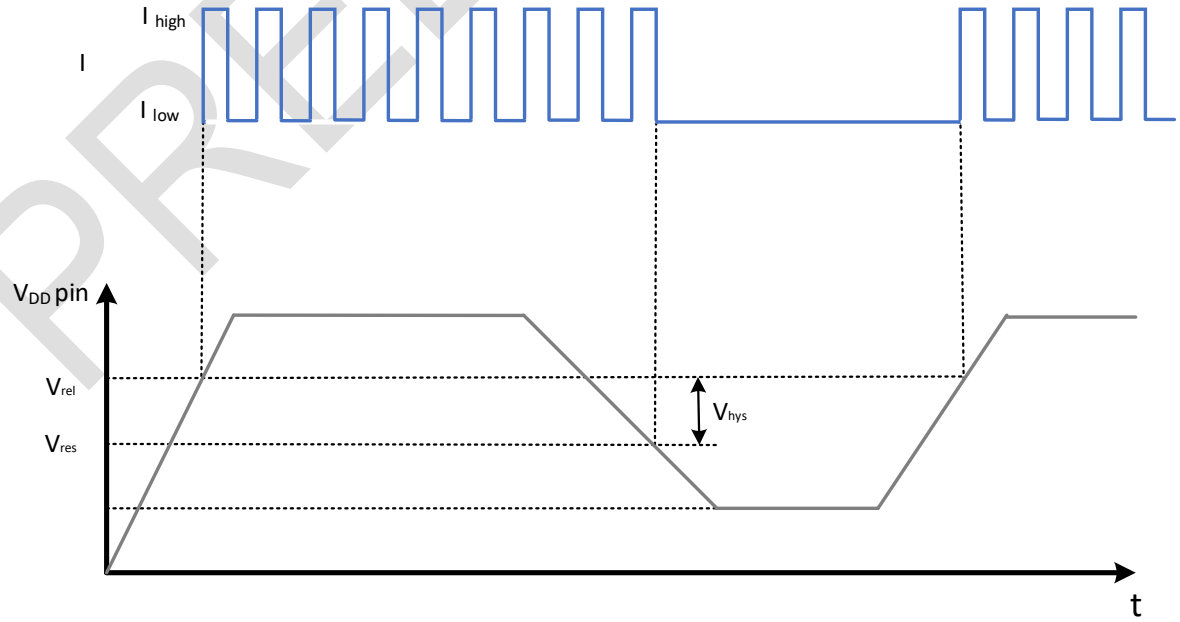


Figure 6 Start-up and under-voltage behavior

4 Specification

4.1 Absolute Maximum Ratings

T_j = – 40℃ to 150℃, 4.5 V ≤ V_{DD} ≤ 20 V if not indicated otherwise.

Parameter	Symbol	Values		Unit	Remarks
		Min.	Max.		
Supply voltage	V_{DD}	-0.3	-	V	T_j < 80°C
		-	20		T_j = 150°C
		-	22		t=10 × 5 min.
		-	24		t=10 × 5 min. R_M ≥ 75 Ω included in V_{DD}
		-	27		t =400 ms, R_M ≥ 75 Ω included in V_{DD}
Reverse polarity voltage	U_{rev}	-22		V	R_M ≥ 75 Ω included in V_{DD}, t < 1h
Reverse polarity current	I_{rev}	-	200	mA	External current limitation required, t < 4 h
			300	mA	External current limitation required, t < 1 h
Junction temperature [1]	T_j				
	EITHER	-40	125		10 h
	OR		150		5000 h
	OR		160		2500 h
	OR		170		500 h
	Additional		190		4 h, V_{DD} < 16.5 V
Number of power-on cycles		500		times	
Immunity to external fields			1	Tesla	Equivalent to 800 kA/m; T_j = -40 to 175°C[2]
Thermal resistance CSO-2	R_{thJA}	-	TBD	K/W	

1) Lifetime parameter to be updated after reliability test complete

2) Conversion: B=μ_0*H (μ_0=4*π*10^{-7}).

4.2 ESD Protections

Tested at room temperature. ESD values below are to be updated after ESD report ready

Parameter	Test Result	Classification level	Notes
HBM	±12kV	AEC-Q100-002, H3B	R = 1.5 kΩ, C =100 pF
CDM	±750 V	AEC-Q100-011, C4	

*All pins

Results below are tested by a leading Tier1 customer.

工作状态	放电位置	放电类型	放电网络	电压等级	功能状态要求	CH503	CH503C
断电	引脚	接触放电	C=150pF,R=330Ω	±4KV	Ⅰ	Pass	Pass
	导体外壳	接触放电	C=150pF,R=330Ω	±6KV	Ⅰ	Pass	Pass

	非导体外壳	空气放电	C=330pF,R=2kΩ	±8KV	Ⅰ	Pass	Pass
通电	传导位置	接触放电	C=150pF,R=330Ω	±8KV	Ⅰ	Pass	Pass
	传导与非传导位置	空气放电	C=330pF,R=2kΩ	±8KV	Ⅰ	Pass	Pass
			C=330pF,R=2kΩ	±20KV	Ⅲ	Pass	Pass

4.3 Operating Range

All parameters specified refer to these operating conditions unless otherwise noticed.

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Supply voltage	V_{DD}	4.5	20	V	Directly on IC leads; includes not thevoltage drop at R_M
	Extended Range	20	24[1)]	V	
Supply voltage modulation	V_{AC}	-	6	Vpp	V_{DD} = 13 V, 0 < f_{mod} <150 kHz[2)]
Junction temperature[3)]	T_j			°C	
	EITHER	-40	125		10 h
	OR		150		5000 h
	OR		160		2500 h
	OR		170		500 h
Pre-induction	B_0	-500	+500	mT	
Pre-induction offset between outer probes	ΔBstat., l/r	-30	+30	mT	
Differential Induction	ΔB	-120	+120	mT	
Magnetic signal frequency	$f$mag	1	10000	Hz	

1) Extended range of 20~24 V is not recommended. Latch-up test with factor 1.5 is not covered. See max ratings also.
2) Sin wave
3) Lifetime parameter to be updated after reliability test complete

4.4 Electrical Characteristics *(to be updated)*

[1)]All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise noticed. Typical values correspond to V_{DD}=12V and T_A=25°C

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Supply current	I_{Low}	5.9	7	8.4	mA	
	I_{High}	11.8	14	16.8	mA	
Supply current ratio	I_{High}/I_{Low}	1.9	2.1	2.3		
Output rise/fall slew rate	t_r, t_f	8 8	– –	22 26	mA/µs	R_M = 75 Ω +/-5% T_j < 125°C T_j < 170°C

Line regulation	dI_x/dV_{DD}			90	µA/V	quasi static[2)]
Initial calibration delay time	$t_{d,input}$	–	120	300	µs	Additional to $n$start[3)2)]
Power up time			210	273	us	*4)2)*
Magnetic edges requiredfor offset calibration	n_{start}	–	–	4	magn. edges	5th edge correct[5)2)]
Number of edges in uncalibrated mode	$n_{DZ\text{-}Startup}$	–	–	4	edges	2)
Number of edges suppressed				0		after power on or reset
Magnetic edges requiredfor first output pulse		1		2		after power on or reset
Duty cycle	*DC*	40	50	60	%	@ΔB ≥ 2 mT sine wave
Signal frequency	*f*	1 2500	– –	2500 10000	Hz	*7)*
Jitter, 1 Hz < f_{mag} < 2.5kHz T_j < 150°C T_j < 170°C	$S_{Jit\text{-}close}$	– –	– –	± 2 ± 3	%	1σ value V_{DD} = 12 V, ΔB ≥ 2 mT[2)]
Jitter, 2.5kHz < f_{mag} < 10kHz T_j < 150°C T_j < 170°C	$S_{Jit\text{-}close}$	– –	– –	± 3 ± 4.5	%	1σ value V_{DD} = 12 V, ΔB ≥ 2 mT[2)]
Jitter, 1 Hz < f_{mag} < 2.5kHz T_j < 150°C T_j < 170°C	$S_{Jit\text{-}far}$	– –	– –	± 4 ± 6	%	1σ value V_{DD} = 12 V 2 mT ≥ ΔB > ΔBLimit[2)]
Jitter, 2.5kHz < f_{mag} < 10kHz T_j < 150°C T_j < 170°C	$S_{Jit\text{-}far}$	– –	– –	± 6 ± 9	%	1σ value V_{DD} = 12 V 2 mT ≥ ΔB > ΔBLimit[2)]
Jitter at board net ripple f_{mag}<10kHz	$S_{Jit\text{-}AC}$			± 0.5	%	*V_{DD} = 13 V ± 6 V_{pp}* *0 < f_{mod} < 150 kHz, ΔB = 15 mT*[2) 8)]
Permitted time for edge to exceed $\Delta\hat{B}_{startup}$	$\Delta t_{startup}$	–	–	590	ms	2)
Time before chip reset[9)]	Δt_{Reset}	590	–	848	ms	2)
Signal behavior after Undervoltage or standstill > t_{Reset} Number of magnetic edges where the first switching occur	$n_{DZ\text{-}Start}$	1	–	2	edge	Magnetic edge amplitudeaccording to $\Delta\hat{B}_{startup}$. $t_{d,input}$ has to be taken into account[2)10)]
Systematic phase error of output edges during start-up and uncalibrated mode		-90	–	+90	°	Systematical phase error of “uncal”edge; nth vs. n + 1st edge (does not include random phase error)

Phase shift change during transition from uncalibrated to calibrated mode	$\Delta\Phi_{switch}$	-45 -90	–	+45 +90	°	2) $dB_{pp} > 4*dB_{startup}$ $dB_{pp} < 4*dB_{startup}$

1) All parameters refer to Test Circuit session.
2) Verified by design/characterization.
3) Occurrence of "Initial calibration delay time $t_{d,input}$"
4) If there is no input signal (standstill), a new initial calibration is triggered each Δt_{Reset}. This calibration has a duration $t_{d,\ input}$ of max. 300 µs. No input signal change is detected during that initial calibration time. In normal operation (signal startup) the probability of t_d, input to come into effect is: $t_{d,\ input}$/time frame for new calibration 300 µs/700 ms = 0.05%. After IC resets (e.g. after a significant undervoltage) $t_{d,\ input}$ will always come into effect.
5) V_{DD} >= 4.5V
6) One magnetic edge is defined as a monotonic signal change of more than 3.3 mT
7) During fast offset alterations, due to the calibration algorithm, exceeding the specified duty cycle is permitted for short time periods
8) Frequency behavior not subject to production test - verified by design/characterization. Frequency above 2.5kHz may have influence on jitter performance and magnetic thresholds.
9) Disturbances are sine-wave shaped: 1sigma value
10) When no output switching occurs for t > Δt_{Reset} the sensor is internally reset after each Δt_{Reset} time frame.
11) A loss of edges may occur at high frequencies

4.5 Magnetic Characteristics

1) All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified. Typical values correspond to V_{DD} = 12 V and T_A = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Limit threshold 1 Hz < f_{mag} < 2.5 kHz 2.5 kHz < f_{mag} < 10 kHz	ΔB_{Limit}	0.35	0.7 –	1.5 1.7	mT	2) 3)
Magnetic differential field change necessary for startup 1 Hz < f < 2.5 kHz 2.5 kHz < f < 10 kHz	$\Delta\hat{B}_{startup}$	– 0.7 –	– 1.4 –	– 3.3 3.9	mT	Magnetic field change for startup with the first edge

1) All parameters refer to described test circuit in this document. See Test Circuit session.
2) Magnetic amplitude values, sine magnetic field, limits refer to the 50% criteria. 50% of edges are missing.
3) ΔB_{Limit} is calculated out of measured sensitivity.

4.6 Description of Magnetic Field

The differential field dB is the resulting signal of difference between signal of right and left Hall element, as shown in Figure 7.

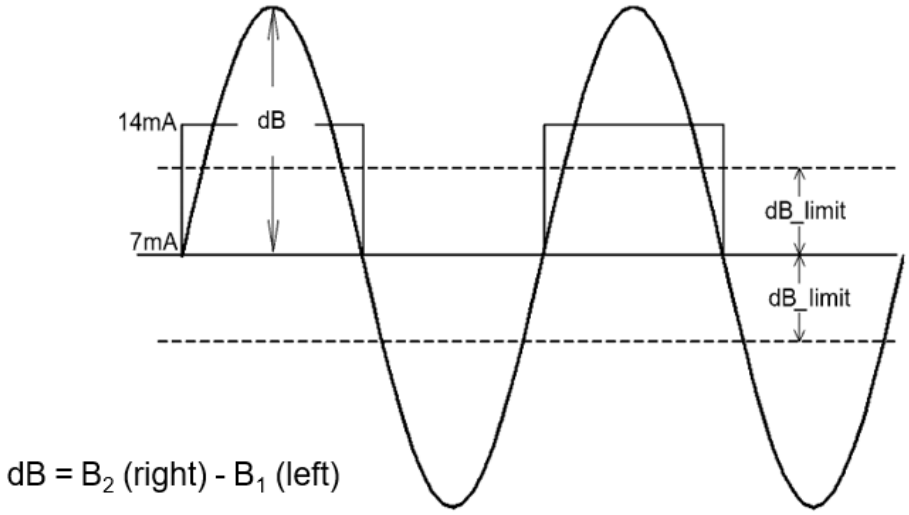


Figure 7 Differential field dB and switching threshold dBlimit (calibrated mode)

The sensor can detect motion of both passive and active wheels. Figure 8 and Figure 9 illustrate the magnetic field definition respectively.

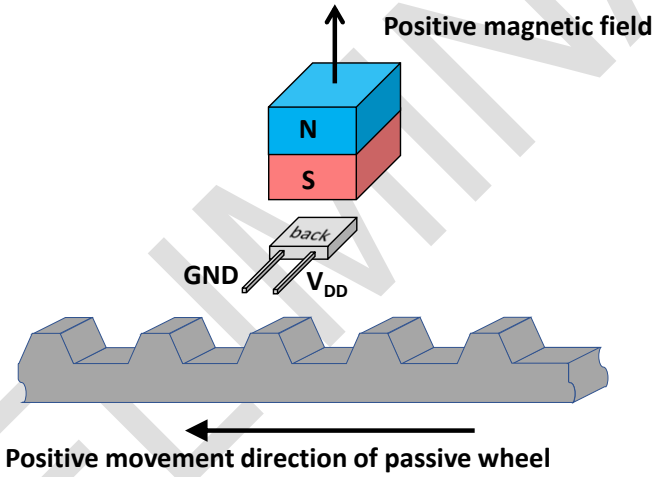


Figure 8 Passive wheels

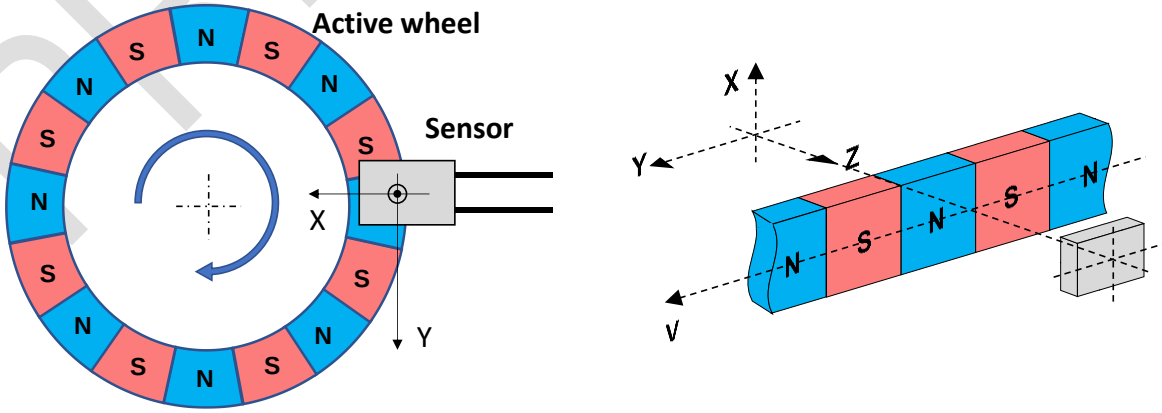


Figure 9 Active wheels

In the passive wheel example, magnetic field is defined as: **"POSITIVE"** is considered, when **SOUTH** pole shows to rear side of the IC housing, or when **NORTH** pole shows to branded side of the IC housing, as shown in Figure 8 and Figure 10.

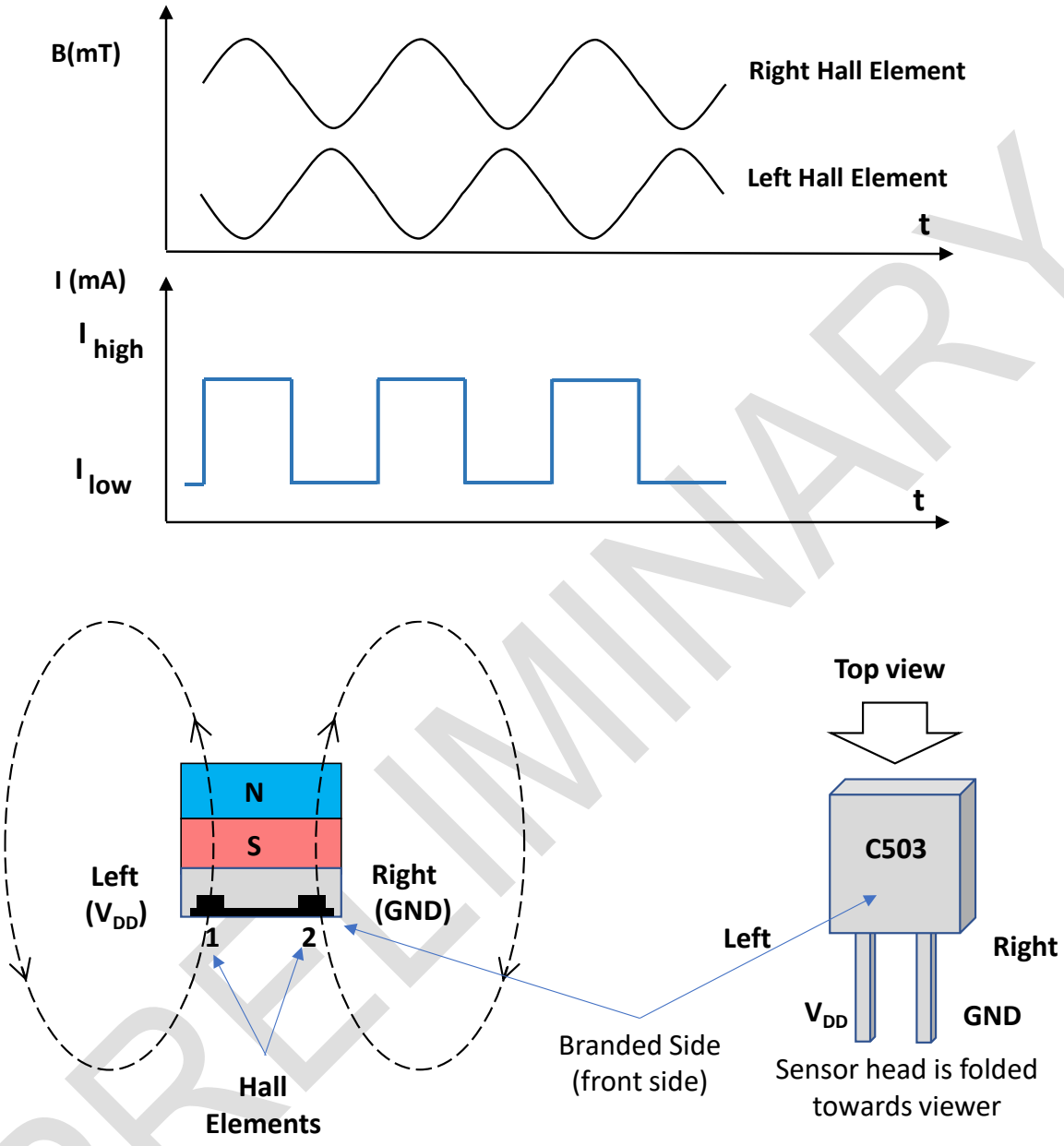


Figure 10 Definition of field direction and sensor switching

5 Application

5.1 Test Circuit

Following test circuit is used for testing and validating electrical parameters.

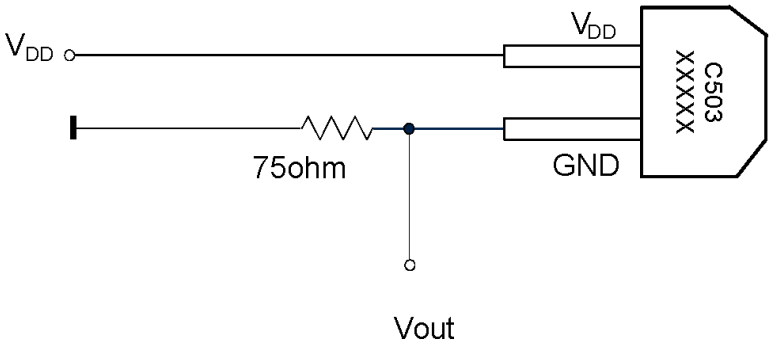


Figure 11 Test Circuit for CH503(C)

5.2 Application Circuit

Circuit below shows the recommended application circuit with reverse bias and overvoltage protection.

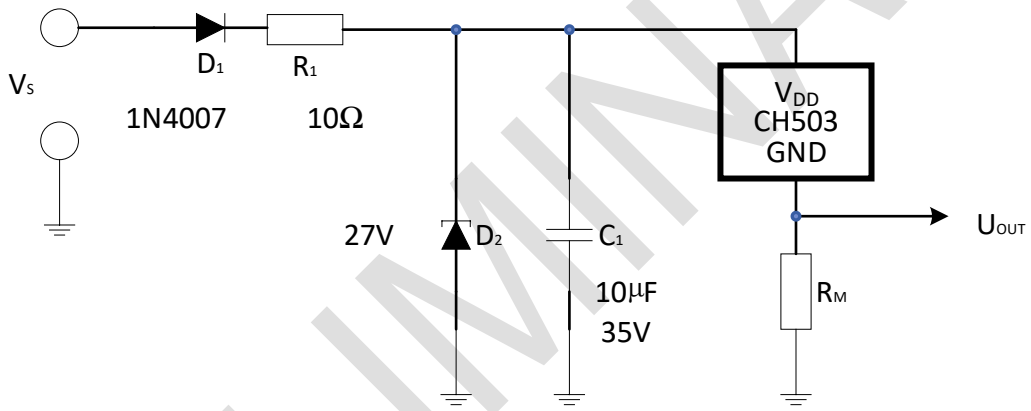


Figure 12 Application Circuit

An implementation of 10 Ω in V_{DD} path reduces minimum power supply direct on leads of the sensor, but decreases max current at D_2 and makes PCB more robust. This PCB represents a compromise of minimum power supply and current flow on D_2. With higher values than 10Ω a higher minimum supply voltage and higher robustness is reached.

5.3 Reference Target Wheel

Air gap measurements and functional tests are done with the target wheel described below. Any other wheel can be used, and the air gap achieved depends on the material, tooth pitch and width of the target wheel.

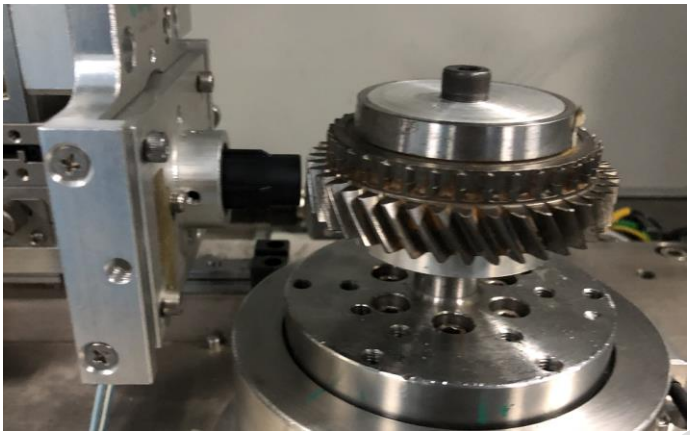


Figure 13 Picture of reference target wheel (number of teeth 41)

5.4 Typical Operating Characteristics

Parameters valid for the described reference target wheel.

Parameter	Symbol	Limit Value			Unit	Remark
		Min	Typ	Max		
Operating Airgap	AG	0.5		*2.1	mm	AG=0 at sensor branded side. Valid at 25°C & 0h. No missing output pulses.

*CH503 & CH503C are still under sampling stage. Parameters can be factory-programmed to adjust max AG.

6 Electro Magnetic Compatibility (EMC)

6.1 EMC Test Circuit

Suggested EMC test circuit, see Figure 13. External components can vary depending on the device version (with or without capacitor inside). Results are dependent on R_M!

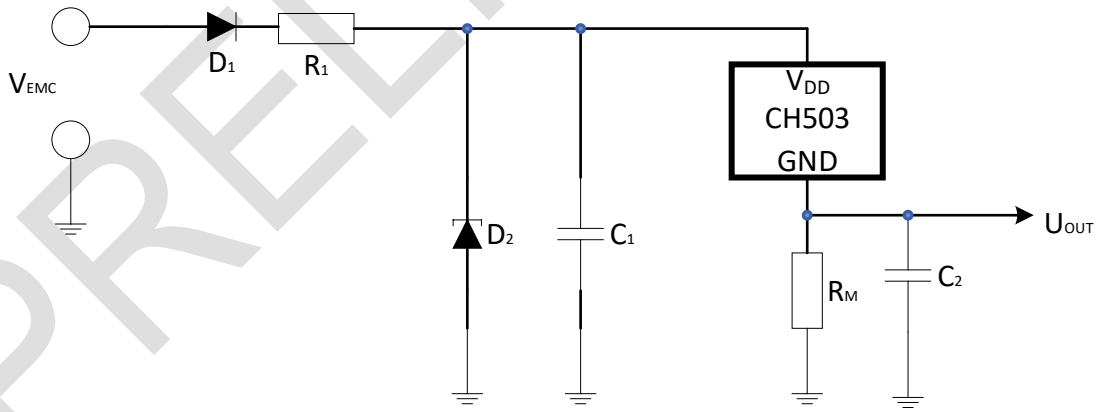


Figure 14 Recommended EMC Test Circuit

Characterization report of EMC on this datasheet are carried out according to Test Circuit in Figure 14, used by a leading sensor Tier1.

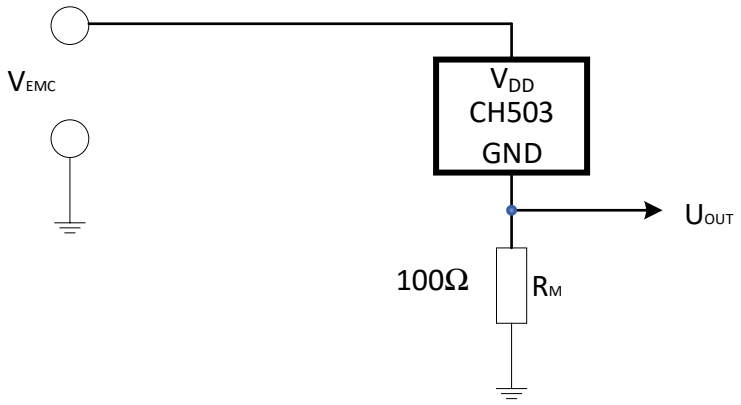


Figure 15 EMC Test Circuit (test circuit by a leading Tier1)

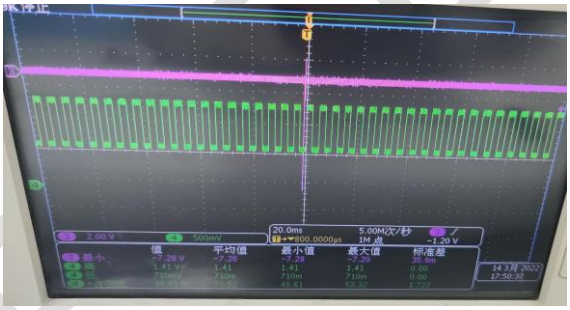
6.2 EMC Results

Test results by a leading Tier1, with test circuit in Figure 14. Both CH503 and CH503C results are given.

6.2.1 Emission

Table EMC – ICC Test Results

测试脉冲	试验等级	脉冲次数	测试等级要求	CH503	CH503C
脉冲c	+5V	600次 (5min)	等级A	测试过程中，信号无异常	
脉冲d	-5V	600次 (5min)	等级A	测试过程中，信号无异常	
脉冲c	+6V	600次 (5min)	等级A	测试过程中，信号无异常	
脉冲d	-6V	600次 (5min)	等级A	测试过程中，信号无异常	
脉冲c	+7V	600次 (5min)	等级A	测试过程中，信号无异常	
脉冲d	-7V	600次 (5min)	等级A	测试过程中，信号无异常	



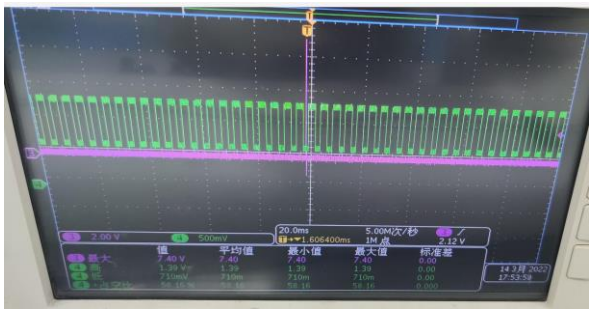
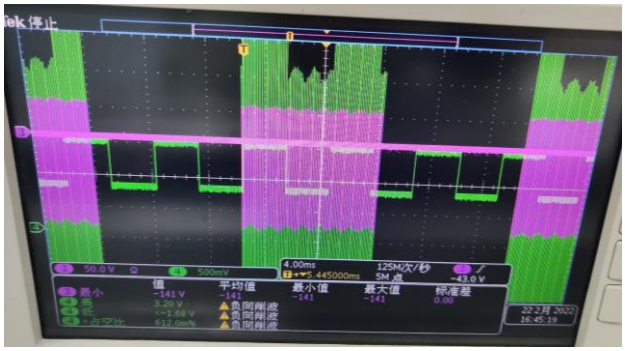
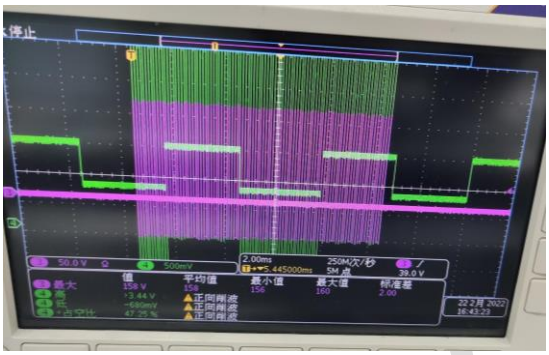


Table EMC – CCC Test Results

测试脉冲	试验等级	脉冲次数	测试等级要求	CH503	CH503C
脉冲a	-80V	10min	等级A	测试过程中，有不影响主波形的耦合现象	
脉冲b	+60V	10min	等级A	测试过程中，有不影响主波形的耦合现象	





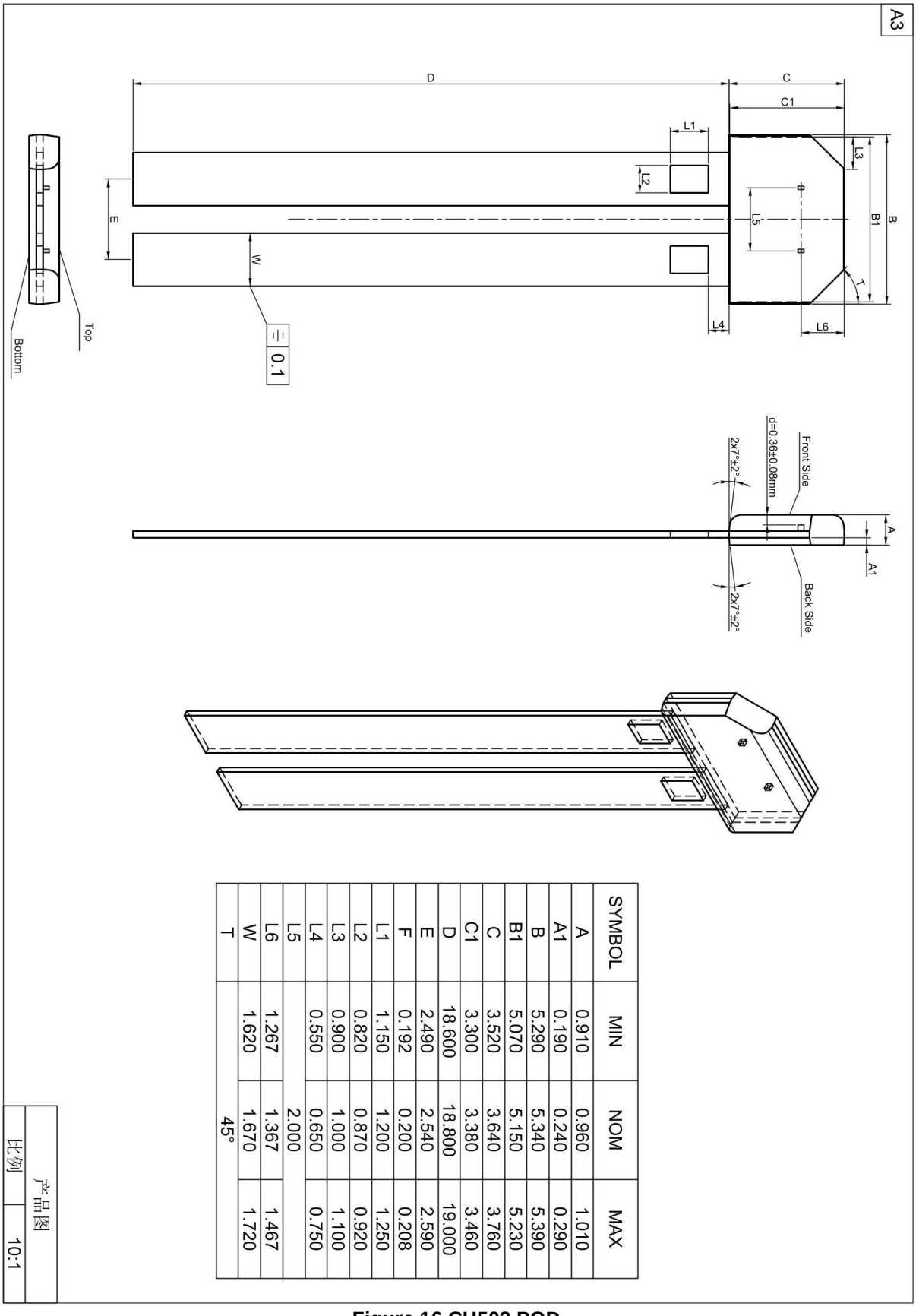
6.2.2 Immunity to radiated disturbances
Table EMC - BCI Test Results

频率（MHz）/ 模式	注入位置	调制	测试等级	要求功能等级	实测功能等级	
					CH503	CH503C
1-400MHz	150mm	CW	等级2 (200mA)	等级A	等级C	等级A
		AM (1kHz,80%)	等级2 (200mA)	等级A	等级C	等级A
		CW	等级1 (100mA)	等级A	等级C	等级A

7 Package Information

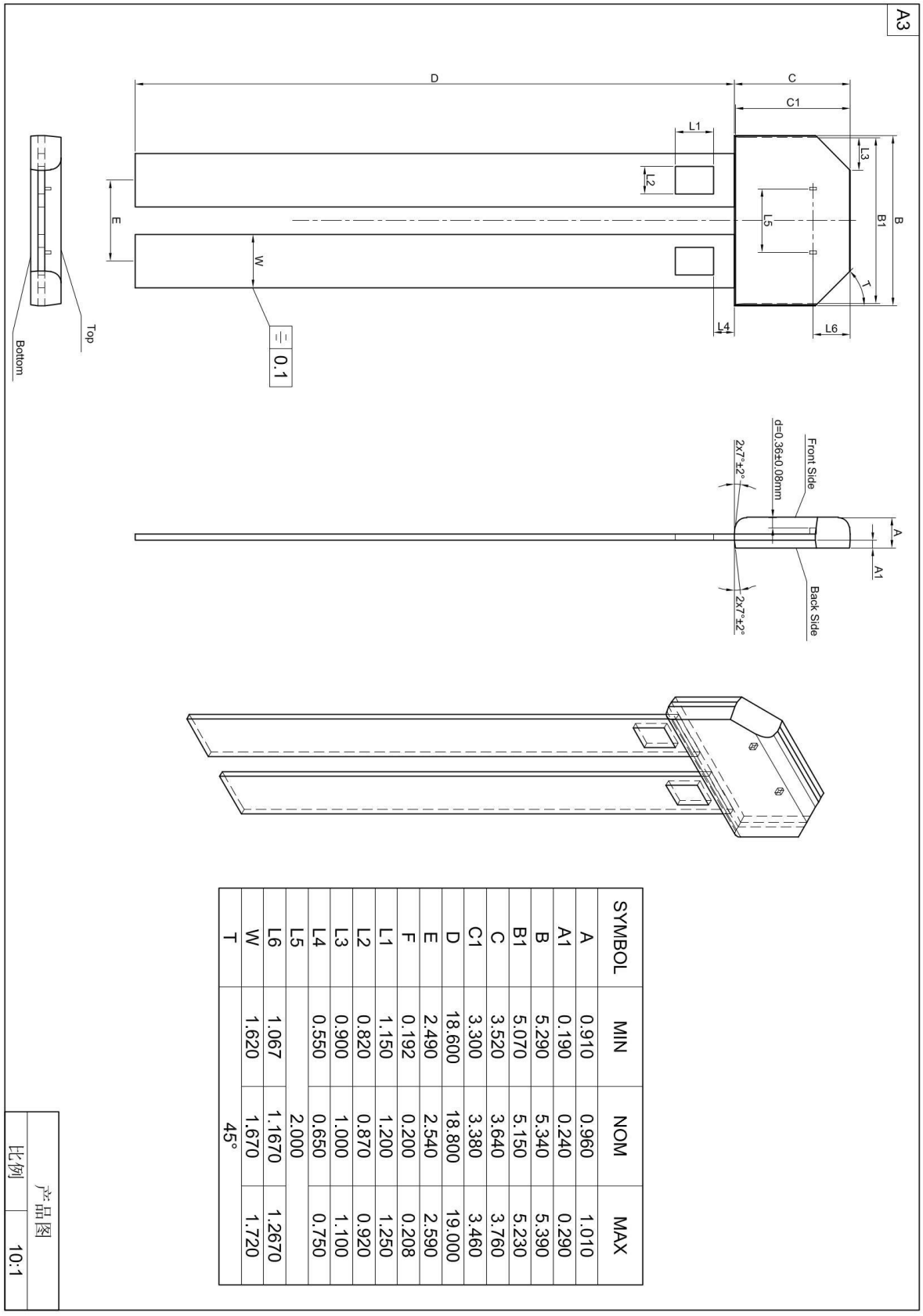
For CH503 and CH503C, the L6 in POD dimension is different.
See details in **Figure 18** and **Figure 19.**

Part Number	Package	Package Dimensions
CH503	CSO-2	Figure 18
CH503C	CSO-2	Figure 19



SYMBOL	MIN	NOM	MAX
A	0.910	0.960	1.010
A1	0.190	0.240	0.290
B	5.290	5.340	5.390
B1	5.070	5.150	5.230
C	3.520	3.640	3.760
C1	3.300	3.380	3.460
D	18.600	18.800	19.000
E	2.490	2.540	2.590
F	0.192	0.200	0.208
L1	1.150	1.200	1.250
L2	0.820	0.870	0.920
L3	0.900	1.000	1.100
L4	0.550	0.650	0.750
L5		2.000	
L6	1.267	1.367	1.467
W	1.620	1.670	1.720
T		45°	

Figure 16 CH503 POD



SYMBOL	MIN	NOM	MAX
A	0.910	0.960	1.010
A1	0.190	0.240	0.290
B	5.290	5.340	5.390
B1	5.070	5.150	5.230
C	3.520	3.640	3.760
C1	3.300	3.380	3.460
D	18.600	18.800	19.000
E	2.490	2.540	2.590
F	0.192	0.200	0.208
L1	1.150	1.200	1.250
L2	0.820	0.870	0.920
L3	0.900	1.000	1.100
L4	0.550	0.650	0.750
L5		2.000	
L6	1.067	1.1670	1.2670
W	1.620	1.670	1.720
T		45°	

Figure 17 CH503C POD